CLAIMS

1. A method of forming a semiconductor structure, the method comprising the steps of:

providing a substrate having a surface oriented on a first crystal plane that enables subsequent crystal planes for channels to be utilized;

forming a first transistor so that a sidewall of a first fin body forms a first channel and so that the sidewall of the first fin body is oriented on a second crystal plane to provide a first carrier mobility; and

forming a second transistor so that a sidewall of a second fin body forms a second channel and so that the sidewall of the second fin body is oriented on a third crystal plane to provide a second carrier mobility that is different from the first carrier mobility.

2. The method of claim 1, wherein the step of providing a substrate comprises the step of providing a silicon substrate having surface oriented on a {110} crystal plane.

3. The method of claim 1, wherein the step of forming a first transistor comprises the step of forming a first transistor so that the sidewall of the first fin body is oriented on a {n n m} plane and n and m are any integer, wherein the step of forming a second transistor comprises forming a second transistor so that the sidewall of the second fin body is oriented on a {a a b} plane and a and b are any integer such that the {n n m} plane and the {a a b} plane are not equivalent by a symmetry transformation.

4. The method of claim 1, wherein the step of forming a first transistor comprises the step of forming one of a first p-channel FinFET (PFET) and a first n-channel FinFET (NFET), wherein the step of forming a second transistor comprises the step of forming one of a second PFET and a second NFET.

5. The method of claim 4, wherein the step of forming one of a first PFET and a first NFET comprises forming one of a first PFET and a first NFET so that the sidewall of the first fin body is oriented on a second crystal plane to provide one of an optimized carrier mobility and a non-optimized carrier mobility, wherein the step of forming one of a second PFET and a second NFET comprises forming one of a second PFET and a second NFET so that the sidewall of the second fin body is oriented on a third crystal plane to provide one of an optimized carrier mobility and a non-optimized carrier mobility.

6. The method of claim 4, wherein the step of forming one of a first PFET and a first NFET comprises forming one of a first PFET and a first NFET so that the sidewall of the first fin body is oriented on one of a {100} crystal plane, a {110} crystal plane, and a {111} crystal plane, wherein the step of forming one of a second PFET and a second NFET comprises forming one of a second PFET and a second NFET so that the sidewall of the second fin body is oriented on one of a {100} crystal plane, a {110} crystal plane, and a {111} crystal plane.

7. A semiconductor structure comprising:

a substrate having a surface oriented on a first crystal plane that enables subsequent crystal planes for channels to be utilized;

a first transistor having a first fin body, the first fin body having a sidewall forming a first channel, the sidewall of the first fin body oriented on a second crystal plane to provide a first carrier mobility; and

a second transistor having a second fin body, the second fin body having a sidewall forming a second channel, the sidewall of the second fin body oriented on a third crystal plane to provide a second carrier mobility that is different from the first carrier mobility.

8. The semiconductor structure of claim 7, wherein the silicon substrate surface is oriented on a {110} crystal plane.

9. The semiconductor structure of claim 7, wherein the sidewall of the first fin body is oriented on a {n n m} plane and n and m are any integer, wherein the sidewall of the second fin body is oriented on a {a a b} plane and a and b are any integer such that the {n n m} plane and the {a a b} plane are not equivalent by a symmetry transformation.

10. The semiconductor structure of claim 7, wherein the first transistor is one of a first p-channel FinFET (PFET) and a first n-channel FinFET (NFET), wherein the second transistor is one of a second PFET and a second NFET.

11. The semiconductor structure of claim 8, wherein the sidewall of the first fin body of one of the first PFET and the first NFET is oriented on a second crystal plane to provide one of an optimized carrier mobility and a non-optimized carrier mobility, wherein the sidewall of the second fin body of one of the second PFET and the second NFET is oriented on a third crystal plane to provide one of an optimized carrier mobility and a non-optimized carrier mobility.

12. The semiconductor structure of claim 8, wherein the sidewall of the first fin body of one of the first PFET and the first NFET is oriented on one of a {100} crystal plane, a {110} crystal plane, and a {111} crystal plane, wherein the sidewall of the second fin body of one of the second PFET and the second NFET is oriented on one of a {100} crystal plane, a {110} crystal plane, and a {111} crystal plane.

13. A semiconductor structure comprising a chip comprising:

a first single crystal semiconductor sidewall channel oriented on a first crystal plane; and

a second single crystal semiconductor sidewall channel oriented on a second crystal plane different from the first crystal plane;

wherein the first crystal plane is not equivalent to the second crystal plane by a symmetry transformation.

14. The semiconductor structure of claim 13, wherein a first mobility is associated with the first crystal plane and a second mobility is associated with the second crystal plane, wherein the first mobility is different from the second mobility.

15. The semiconductor structure of claim 13, wherein the chip has a surface oriented on a {110} crystal plane.

16. The semiconductor structure of claim 13, wherein the first single crystal semiconductor sidewall channel is part of a first FinFET and the second single crystal semiconductor sidewall channel is part of a second FinFET.

17. The semiconductor structure of claim 16, wherein the first FinFET is one of a first p-channel FinFET (PFET) and a first n-channel FinFET (NFET), wherein the second FinFET is one of a second PFET and a second NFET.

18. The semiconductor structure of claim 17, wherein one of the first PFET and the first NFET is oriented on a second crystal plane to provide one of an optimized carrier mobility and a non-optimized carrier mobility, wherein one of the second PFET and the second NFET is oriented on a third crystal plane to provide one of an optimized carrier mobility and a non-optimized carrier mobility.

19. The semiconductor structure of claim 17, wherein one of the first PFET and the first NFET is oriented on one of a {100} crystal plane, a {110} crystal plane, and a {111} crystal plane, wherein one of the second PFET and the second NFET is oriented on one of a {100} crystal plane, a {110} crystal plane, and a {111} crystal plane.

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